IN THE CLAIMS:

The current claims follow. For claims not marked as amended in this response, any difference in the claims below and the previous state of the claims is unintentional and in the nature of a typographical error.

1. (Currently Amended) For use in a router, a routing table search circuit for determining a first destination address for a first received data packet comprising:

a forwarding table comprising a plurality of forwarding table entries, each of said forwarding table entries comprising a destination address;

a trie tree search table for translating a portion of an address associated with said first received data packet into a destination pointer for accessing said first destination address in said forwarding table, wherein a first stage of said trie tree search table is searched using a received address pointer retrieved from a previous stage of said trie tree search table and a first m-bit symbol comprising m bits of said portion;

at least one consecutive identical symbols table associated with said first stage of said trie tree search table; and

a control circuit capable of determining that a second m-bit symbol immediately following said first m-bit symbol is the same as said first m-bit symbol, wherein said control circuit, in response to said determination, determines a total number of consecutive identical m-bit symbols beginning with said first m-bit symbol.

2. (Currently Amended) The routing table search circuit as set forth in Claim 1 wherein said control circuit retrieves from said at least one consecutive identical symbols table a first address pointer determined by said total number of consecutive identical m-bit symbols.

3. (Original) The routing table search circuit as set forth in Claim 2 wherein said first address pointer comprises said destination pointer.

4. (Original) The routing table search circuit as set forth in Claim 2 wherein said first address pointer is used to search a subsequent stage of said trie tree search table.

5. (Currently Amended) The routing table search circuit as set forth in Claim 2 wherein said at least one consecutive identical symbols table comprises a plurality of consecutive identical symbols tables and said control circuit uses a value of said first m-bit symbol to select a first one of said plurality of consecutive identical symbols tables.

6. (Currently Amended) The routing table search circuit as set forth in Claim 5 further comprising an intermediate table for storing a plurality of consecutive identical symbols tables pointers, each of said consecutive identical symbols tables pointers associated with one of said plurality of consecutive identical symbols tables.

7. (Currently Amended) The routing table search circuit as set forth in Claim 6 wherein said control circuit uses said value of said first m-bit symbol to retrieve a first one of said consecutive identical symbols tables pointers from said intermediate table.

8. (Currently Amended) The routing table search circuit as set forth in Claim 7 wherein said control circuit uses said retrieved first identical consecutive symbols tables pointer to select said first consecutive identical symbols table.

9. (Original) The routing table search circuit as set forth in Claim 8 wherein said first address pointer comprises said destination pointer.

10. (Original) The routing table search circuit as set forth in Claim 8 wherein said first address pointer is used to search a subsequent stage of said trie tree search table.

11. (Currently Amended) A router for interconnecting N interfacing peripheral devices, said router comprising:

a switch fabric; and

a plurality of routing nodes coupled to said switch fabric, each of said routing nodes comprising a routing table search circuit for determining a first destination address for a first received data packet, the routing table search circuit comprising:

a forwarding table comprising a plurality of forwarding table entries, each of said forwarding table entries comprising a destination address;

a trie tree search table for translating a portion of an address associated with said first received data packet into a destination pointer for accessing said first destination address in said forwarding table, wherein a first stage of said trie tree search table is searched using a received address pointer retrieved from a previous stage of said trie tree search table and a first m-bit symbol comprising m bits of said portion;

at least one consecutive identical symbols table associated with said first stage of said trie tree search table; and

a control circuit capable of determining that a second m-bit symbol immediately following said first m-bit symbol is the same as said first m-bit symbol, wherein said control circuit, in response to said determination, determines a total number of consecutive identical m-bit symbols beginning with said first m-bit symbol.

12. (Currently Amended) The router as set forth in Claim 11 wherein said control circuit retrieves from said at least one consecutive identical symbols table a first address pointer determined by said total number of consecutive identical m-bit symbols.

13. (Original) The router as set forth in Claim 12 wherein said first address pointer comprises said destination pointer.

14. (Original) The router as set forth in Claim 12 wherein said first address pointer is used to search a subsequent stage of said trie tree search table.

15. (Currently Amended) The router as set forth in Claim 12 wherein said at least one consecutive identical symbols table comprises a plurality of consecutive identical symbols tables and said control circuit uses a value of said first m-bit symbol to select a first one of said plurality of consecutive identical symbols tables.

16. (Currently Amended) The router as set forth in Claim 15 further comprising an intermediate table for storing a plurality of consecutive identical symbols tables pointers, each of said consecutive identical symbols tables pointers associated with one of said plurality of consecutive identical symbols tables.

17. (Currently Amended) The router as set forth in Claim 16 wherein said control circuit uses said value of said first m-bit symbol to retrieve a first one of said consecutive identical symbols tables pointers from said intermediate table.

18. (Currently Amended) The router as set forth in Claim 17 wherein said control circuit uses said retrieved first consecutive identical symbols tables pointer to select said first consecutive identical symbols table.

19. (Original) The router as set forth in Claim 18 wherein said first address pointer comprises said destination pointer.

20. (Original) The router as set forth in Claim 18 wherein said first address pointer is used to search a subsequent stage of said trie tree search table.

21. (Currently Amended) For use in router, a method for determining a first destination address for a first received data packet comprising the steps of:

searching a first stage of trie tree search table using a received address pointer retrieved from a previous stage of the trie tree search table and a first m-bit symbol comprising m bits of a portion of an address associated with the first received data packet;

determining that a second m-bit symbol immediately following the first m-bit symbol is the same as the first m-bit symbol;

in response to the determination, determining a total number of consecutive identical m-bit symbols beginning with the first m-bit symbol; and

retrieving from a consecutive identical symbols table associated with the first stage of the trie tree search table a first address pointer determined by the total number of consecutive identical m-bit symbols, wherein the first address pointer may be used to access the first destination address in a forwarding table of the router.

22. (Original) The method as set forth in Claim 21 further comprising the step of accessing the first destination address in the forwarding table using the first address pointer.

23. (Original) The method as set forth in Claim 21 further comprising the step of searching a subsequent stage of the trie tree search table using the first address pointer.

24. (Currently Amended) The method as set forth in Claim 21 wherein the consecutive identical symbols table comprises a plurality of consecutive identical symbols tables and further comprising the step of selecting a first one of the plurality of consecutive identical symbols tables according to a value of the first m-bit symbol.